

20-Bit, Stereo A/D Converter for Digital Audio

Features

- CS5334
Dynamic Range: 100 dB
THD+N: -90 dB
- CS5335
Dynamic Range: 105 dB
THD+N: -95 dB
- 128X Oversampling
- Fully Differential Inputs
- Linear Phase Digital Anti-Alias Filtering
21.7 kHz passband ($f_s = 48\text{kHz}$)
85 dB stop band attenuation
0.0025 dB pass band ripple
- High Pass Filter - DC offset removal
- Peak Signal Level Detector
High Resolution and Bar Graph Modes

General Description

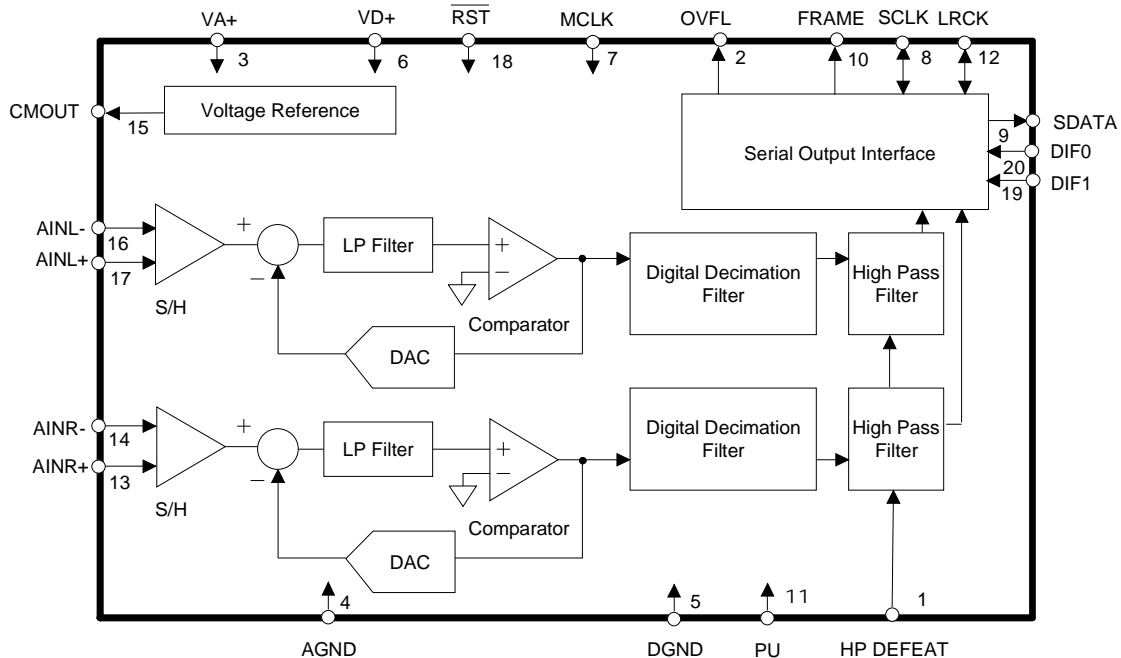
The CS5334 and CS5335 are 2-channel, single +5V supply, pin compatible analog-to-digital converters for digital audio systems. The CS5334 and CS5335 perform sampling, analog-to-digital conversion and anti-alias filtering, generating 20-bit values for both left and right inputs in serial form. The output word rate can be up to 50 kHz per channel.

The CS5334 and CS5335 use 4th-order, delta-sigma modulation with 128X oversampling followed by digital filtering and decimation, which removes the need for an external anti-alias filter. These ADCs use a differential architecture which provides excellent noise rejection.

The CS5334 and CS5335 have a filter passband to 21.7kHz. The filter has linear phase, 0.0025 dB pass-band ripple, and >85 dB stopband rejection. An on-chip high pass filter is also included to remove DC offsets.

ORDERING INFORMATION:

Model	Temp. Range	Package Type
CS5334-KS	-10° to 70°C	20-pin Plastic SSOP
CS5335-KS	-10° to 70°C	20-pin Plastic SSOP



Preliminary Product Information

This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

ANALOG CHARACTERISTICS ($T_A = 25^\circ\text{C}$; $V_{A+} = V_{D+} = 5\text{V}$; -1 dBFS Input Sinewave, 997 Hz; $F_s = 48\text{ kHz}$; $MCLK = 12.288\text{ MHz}$; $SCLK = 3.072\text{ MHz}$; Measurement Bandwidth is 10 Hz to 20 kHz unless otherwise specified; Logic 0 = 0V, Logic 1 = V_{D+})

Parameter	Symbol	CS5334			CS5335			Units	
		Min	Typ	Max	Min	Typ	Max		
Resolution		20	-	-	20	-	-	Bits	
Dynamic Performance									
Dynamic Range	A-weighted	TBD	100	-	TBD	105	-	dB	
		TBD	97	-	TBD	102	-		
Total Harmonic Distortion + Noise	-1 dB	THD+N	-	-90	TBD	-	-95	TBD	dB
	-20 dB		-	-77	TBD	-	-82	TBD	dB
	-60 dB		-	-37	TBD	-	-42	TBD	dB
Interchannel Phase Deviation		-	0.01	-	-	0.01	-	Degree	
Interchannel Isolation	(dc to 20 kHz)	-	100	-	-	105	-	dB	
dc Accuracy									
Interchannel Gain Mismatch		-	0.05	-	-	0.05	-	dB	
Gain Error		-	-	± 5	-	-	± 5	%	
Gain Drift		-	200	-	-	200	-	ppm/ $^\circ\text{C}$	
Offset Error	with HPF	-	0	-	-	0	-	LSB	
	HP defeat with CAL	-	+/-	-	-	+/-	-	LSB	
			100			100			
Analog Input									
Input Voltage Range	(Differential)	V_{IN}	1.9	2.0	2.1	1.9	2.0	2.1	V_{rms}
Input Impedance		Z_{IN}	-	30	-	-	30	-	$k\Omega$
Input Bias Voltage			-	2.2	-	-	2.2	-	V
Power Supplies									
Power Supply Current	I_A	-	38	TBD	-	40	TBD	mA	
	I_D	-	25	TBD	-	25	TBD	mA	
	Power Down (I_A+I_D)	-	0.2	-	-	0.2	-	mA	
Power Dissipation	Normal	-	315	TBD	-	325	TBD	mW	
	Power Down	-	1.0	-	-	1.0	-	mW	
Power Supply Rejection Ratio		-	50	-	-	55	-	dB	

Specifications are subject to change without notice

DIGITAL FILTER CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$; $V_{A+} = V_{D+} = 5V \pm 5\%$; $F_s = 48\text{ kHz}$)

Parameter	Symbol	Min	Typ	Max	Units
Passband (Note 1)		0.02	-	21.7	kHz
Passband Ripple		-	-	± 0.0025	dB
Stopband (Note 1)		26.3	-	6118	kHz
Stopband Attenuation (Note 2)		85	-	-	dB
Group Delay ($F_s = \text{Output Sample Rate}$)	t_{gd}	-	$32/F_s$	-	s
Group Delay Variation vs. Frequency	Δt_{gd}	-	-	0	μs
High Pass Filter Characteristics					
Frequency Response: -3 dB (Note 1)		-	0.9	-	Hz
-0.01 dB		-	20	-	Hz
Phase Deviation @ 20 Hz (Note 1)		-	2.6	-	Degree
Passband Ripple		-	-	0	dB

- Notes:
1. Filter characteristic scales with output sample rate.
 2. The analog modulator samples the input at 6.144 MHz for an output sample rate of 48 kHz. There is no rejection of input signals which are multiples of the sampling frequency ($n \times 6.144\text{ MHz} \pm 21.7\text{kHz}$ where $n = 0, 1, 2, 3, \dots$).

DIGITAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$; $V_{A+} = V_{D+} = 5V \pm 5\%$)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	2.4	-	-	V
Low-Level Input Voltage	V_{IL}	-	-	0.8	V
High-Level Output Voltage at $I_o = -20\text{ }\mu\text{A}$	V_{OH}	$(V_{D+}) - 1.0$	-	-	V
Low-Level Output Voltage at $I_o = 20\text{ }\mu\text{A}$	V_{OL}	-	-	0.4	V
Input Leakage Current	I_{in}	-	-	10	μA

ABSOLUTE MAXIMUM RATINGS ($AGND = 0V$, all voltages with respect to ground.)

Parameter	Symbol	Min	Typ	Max	Units
DC Power Supply:	V_{A+}	-0.3	-	+6.0	V
Input Current, Any Pin Except Supplies (Note 3)	I_{in}	-	-	± 10	mA
Analog Input Voltage (Note 4)	V_{INA}	-0.7	-	$(V_{A+}) + 0.7$	V
Digital Input Voltage (Note 4)	V_{IND}	-0.7	-	$(V_{A+}) + 0.7$	V
Ambient Temperature (power applied)	T_A	-55	-	+125	$^\circ\text{C}$
Storage Temperature	T_{stg}	-65	-	+150	$^\circ\text{C}$

- Notes:
3. Any Pin except supplies. Transient currents of up to $\pm 100\text{ mA}$ on the analog input pins will not cause SCR latch-up.
 4. The maximum over/under voltage is limited by the input current.

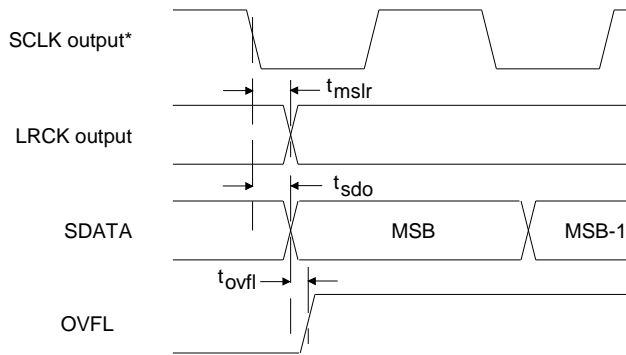
WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

SWITCHING CHARACTERISTICS

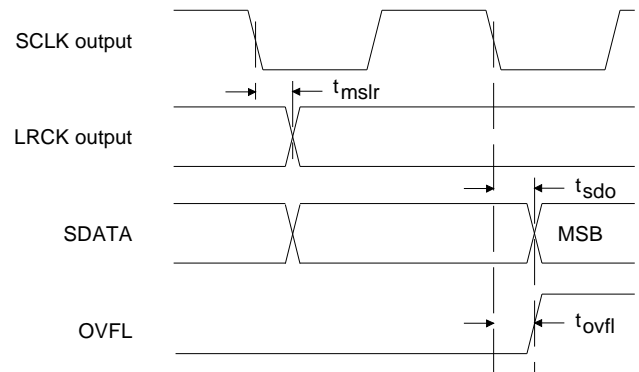
(T_A = 25 °C; V_{A+} = 5V ± 5%; Inputs: Logic 0 = 0V, Logic 1 = V_{A+} = V_{D+}; C_L = 20 pF)

Parameter	Symbol	Min	Typ	Max	Units
Output Sample Rate	F _s	2.0	-	50	kHz
MCLK Period	MCLK / LRCK = 256 t _{clkw}	78	-	1953	ns
MCLK Low	MCLK / LRCK = 256 t _{ckl}	31	-	-	ns
MCLK High	MCLK / LRCK = 256 t _{ckh}	31	-	-	ns
MCLK Period	MCLK / LRCK = 384 t _{clkw}	52	-	1302	ns
MCLK Low	MCLK / LRCK = 384 t _{ckl}	20	-	-	ns
MCLK High	MCLK / LRCK = 384 t _{ckh}	20	-	-	ns
MCLK Period	MCLK / LRCK = 512 t _{clkw}	39	-	976	ns
MCLK Low	MCLK / LRCK = 512 t _{ckl}	15	-	-	ns
MCLK High	MCLK / LRCK = 512 t _{ckh}	15	-	-	ns
MASTER MODE					
SCLK falling to LRCK	(Note 5) t _{mslr}	-10	-	10	ns
SCLK falling to SDATA valid	(Note 5) t _{sdo}	-10	-	35	ns
SCLK Duty cycle		-	50	-	%
SCLK falling to Frame Valid	(Note 5) t _{sfo}	-10	-	(Note 6)	ns
LRCK edge to OVFL Valid	t _{ovfl}	-10	-	30	ns
LRCK edge to OVFL edge delay	t _{ovfl}	-10	-	(Note 10)	ns
SLAVE MODE					
LRCK duty cycle		25	50	75	%
SCLK Period	t _{sclkw}	(Note 7)	-	-	ns
SCLK Pulse Width Low	(Note 8) t _{sckl}	(Note 11)	-	-	ns
SCLK Pulse Width High	(Note 9) t _{sckh}	50	-	-	ns
SCLK falling to SDATA valid	(Note 5) t _{dss}	-	-	(Note 11)	ns
LRCK edge to MSB valid	t _{lrdss}	-	-	(Note 11)	ns
SCLK rising to LRCK edge delay	(Note 12) t _{slr1}	50	-	-	ns
LRCK edge to rising SCLK setup time	(Note 12) t _{slr2}	(Note 11)	-	-	ns
SCLK falling to Frame delay	t _{sfo}	-	-	(Note 13)	ns

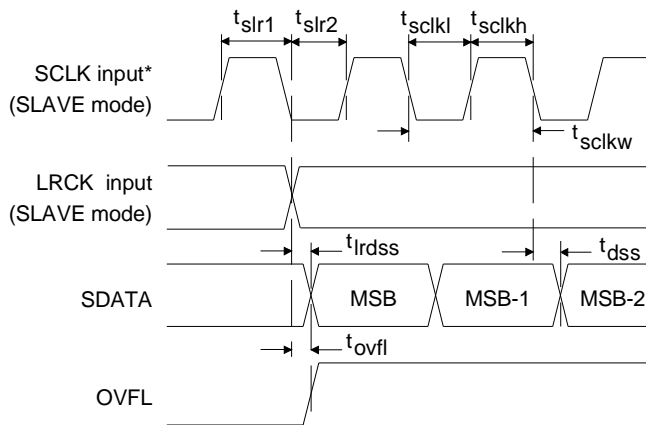
- Notes: 5. SCLK rising for Mode 1. 6. $\frac{1}{(1024)(F_s)} + 30\text{ns}$ 7. $\frac{1}{(96)(F_s)}$ 8. Pulse Width High for Mode 1
9. Pulse Width Low for Mode 1 10. $\frac{1}{(512)(F_s)} + 20\text{ns}$ 11. $\frac{1}{(512)(F_s)} + 50\text{ns}$
12. SCLK Falling for Mode 1 13. $\frac{1}{(384)(F_s)} + 35\text{ns}$



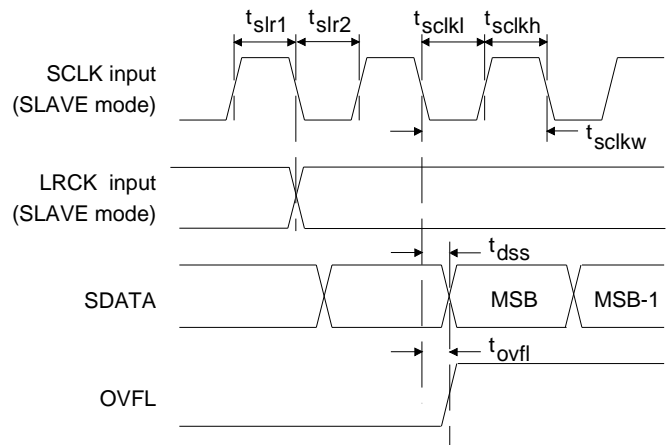
**SCLK to SDATA & LRCK - MASTER mode
Format 0 and 1**



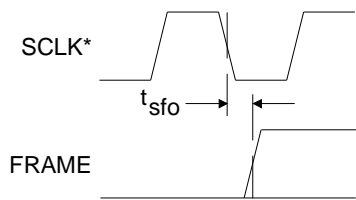
**SCLK to SDATA & LRCK - MASTER mode
Format 2**



**SCLK to LRCK & SDATA - SLAVE mode
Format 0 & 1**



**SCLK to LRCK & SDATA - SLAVE mode
Format 2**



SCLK to Frame Delay

*SCLK is inverted for Format 1

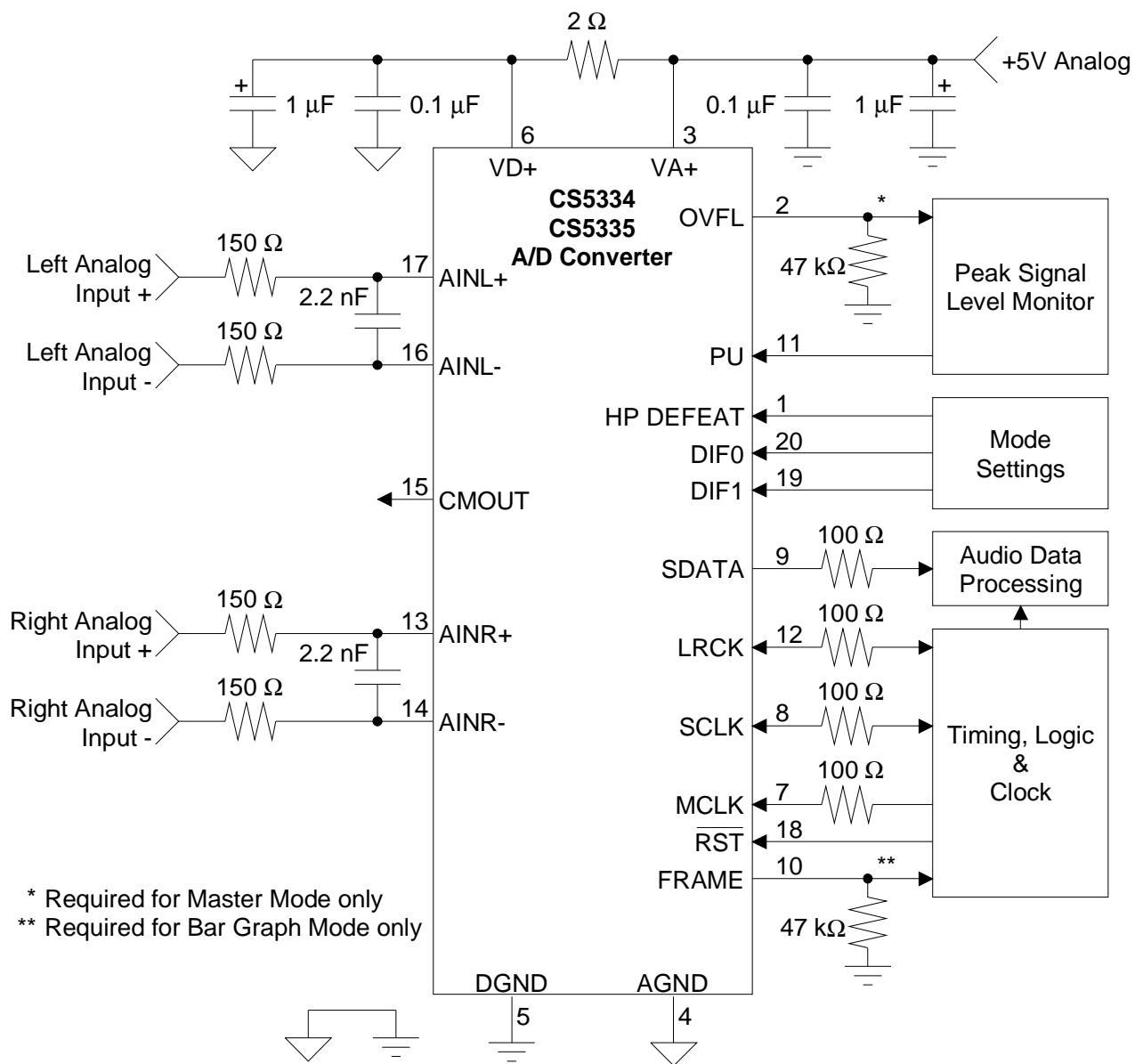


Figure 1. Typical Connection Diagram

SYSTEM DESIGN

The CS5334 and CS5335 are 20-bit, 2-channel Analog-to-Digital Converters designed for digital audio applications. These devices use two one-bit delta-sigma modulators which simultaneously sample the analog input signals at 128 times the output sample rate (F_s). The resulting serial bit streams are digitally filtered, yielding a pair of 20-bit values. This technique yields nearly ideal conversion performance independent of input frequency and amplitude. The converter does not require difficult-to-design or expensive anti-alias filters and does not require external sample-and-hold amplifiers or a voltage reference. Very few external components are required to support these ADCs. Normal power supply decoupling components and a resistor and capacitor on each input for anti-aliasing are all that's required, as shown in Figure 1.

An on-chip voltage reference provides for a differential input signal range of 2.0 Vrms. Output data is available in serial form, coded as 2's complement, 20-bit numbers. Typical power consumption is 325 mW which can be reduced to 1.0 mW using the power-down feature.

Master Clock

The master clock (MCLK) is the clock source for the delta-sigma modulator sampling and digital filters. In Master Mode, the frequency of this clock must be $256 \times F_s$. In Slave Mode, the master clock must be either $256 \times$, $384 \times$ or $512 \times F_s$. Table 1 shows some common master clock frequencies.

LRCK (kHz)	MCLK (MHz)		
	256 X	384 X	512 X
32	8.1920	12.2880	16.3840
44.1	11.2896	16.9344	22.5792
48	12.2880	18.4320	24.5760

Table 1. Common Clock Frequencies

SERIAL DATA INTERFACE

The CS5334 and CS5335 support three serial data formats, including I²S, which are selected via the digital input format pins DIF0 and DIF1. The digital input format determines the relationship between the serial data, left/right clock and serial clock. Table 2 lists the three formats, along with the associated figure number. The serial data interface is accomplished via the serial data output, SDATA, serial data clock, SCLK, and the left/right clock, LRCK.

DIF1	DIF0	FORMAT	FIGURE
0	0	0	3
0	1	1	4
1	0	2	5
1	1	power-down	-

Table 2. Digital Input Formats

Serial Data

The serial data block consists of 20 bits of audio data presented in 2's-complement format with the MSB-first, followed by 4 bits of zero and 8 Peak Signal Level, PSL, bits as shown in Figure 2. The data is clocked from SDATA by the serial clock and the channel is determined by the Left/Right clock.

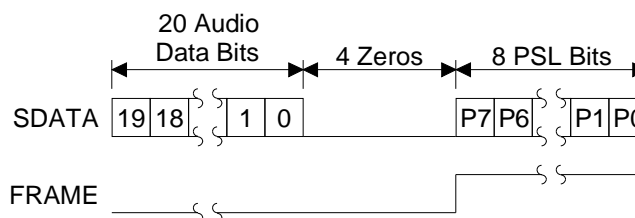


Figure 2. Data Block and Frame

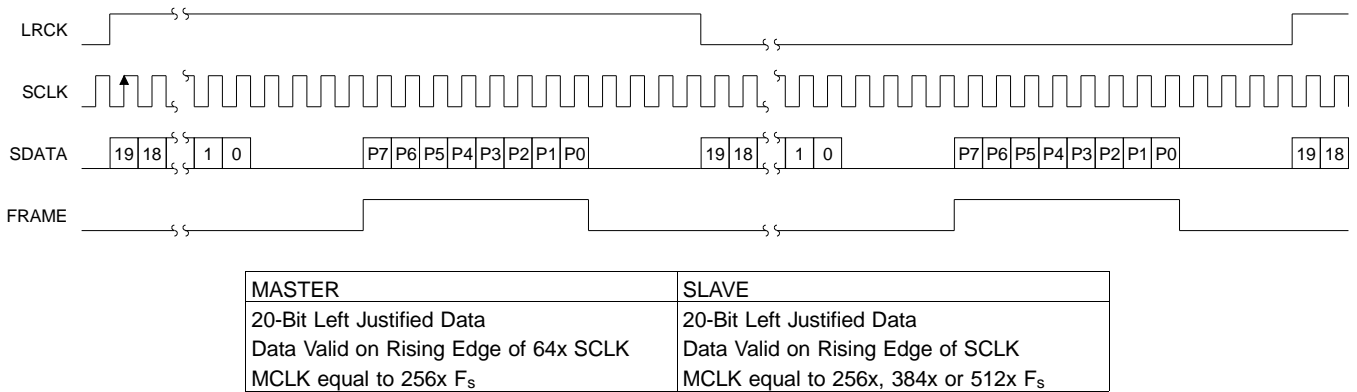


Figure 3. Serial Data Format 0

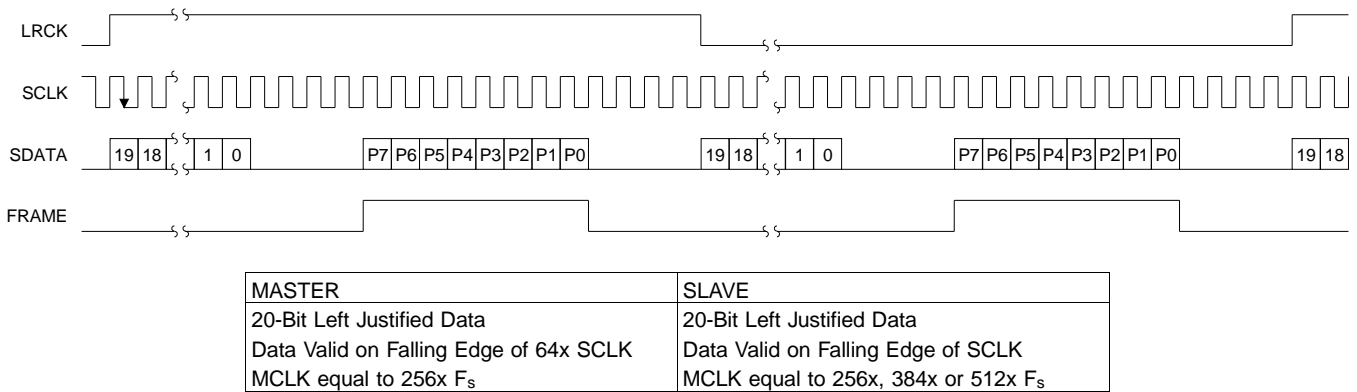


Figure 4. Serial Data Format 1

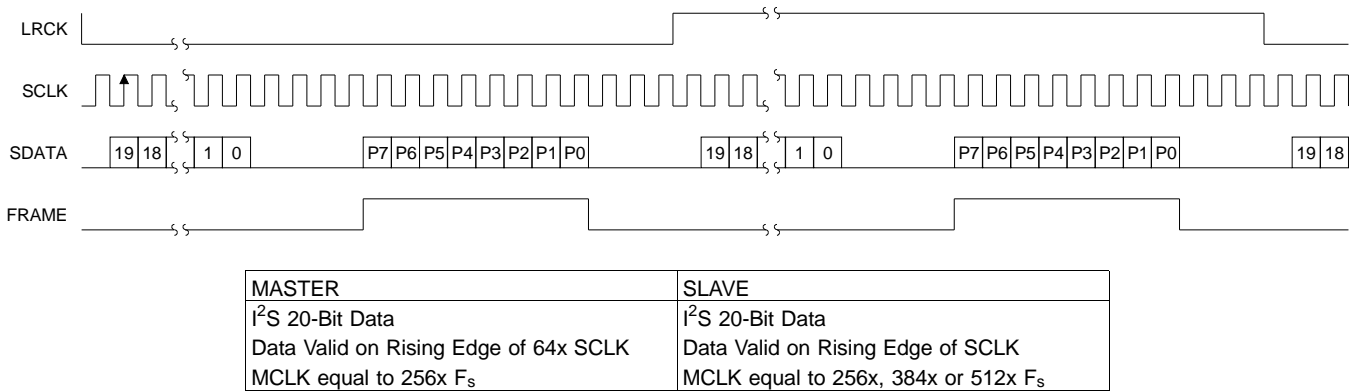


Figure 5. Serial Data Format 2

Serial Clock

The serial clock shifts the digitized audio data from the internal data registers via the SDATA pin. SCLK is an output in Master Mode. Internal dividers will divide the master clock by 4 to generate a serial clock which is $64 \times F_s$. In Slave Mode, SCLK is an input with a serial clock typically between $48 \times$ and $128 \times F_s$. However, the serial clock must be a minimum of $64 \times F_s$ to access the Peak Signal Level bits.

Left / Right Clock

The Left/Right clock determines which channel, left or right, is to be output on SDATA. Although the outputs for each channel are transmitted at different times, Left/Right pairs represent simultaneously sampled analog inputs. In Master Mode, LRCK is an output whose frequency is equal to F_s . In Slave Mode, LRCK is an input whose frequency must be equal to the output sample rate, F_s .

Master Mode

In Master mode, SCLK and LRCK are outputs which are internally derived from the Master Clock. Internal dividers will divide MCLK by 4 to generate a SCLK which is $64 \times F_s$ and by 256 to generate a LRCK which is equal to F_s . Master mode is only supported with a $256 \times$ master clock. The CS5334/5 is placed in the Master mode with a $47 \text{ k}\Omega$ pull-down resistor on the OVFL pin.

Slave Mode

LRCK and SCLK become inputs in SLAVE mode. LRCK must be externally derived from MCLK and be equal to F_s . The serial clock is typically between $64 \times$ and $128 \times F_s$. A $48 \times F_s$ serial clock is possible though will not allow access to the Peak Signal Level bits. Master clock frequencies of $256 \times$, $384 \times$ and $512 \times F_s$ are supported. The ratio of the applied master clock to the left/right clock is automatically detected dur-

ing power-up and internal dividers are set to generate the appropriate internal clocks.

Analog Connections

Figure 1 shows the analog input connections. The analog inputs are presented to the modulators via the AINR+/- and AINL+/- pins. Each analog input pin will accept a maximum of 1 Vrms centered at +2.2 Volt as shown in Figure 6. Input signals can be AC or DC coupled and the CMOUT output may be used as a reference for DC coupling. However, CMOUT is not buffered and the maximum current is $10 \mu\text{A}$.

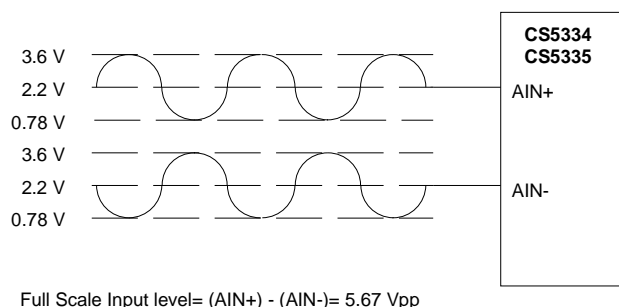


Figure 6. Full Scale Input Levels

The CS5334 and CS5335 sample the analog inputs at $128 \times F_s$, 6.144 MHz for a 48 kHz sample-rate. The digital filter rejects all noise above 26.3 kHz except for frequencies right around 6.144 MHz \pm 21.7 kHz (and multiples of 6.144 MHz). Most audio signals do not have significant energy at 6.144 MHz. Nevertheless, a 150Ω resistor in series with each analog input and a 2.2 nF capacitor across the inputs will attenuate any noise energy at 6.144 MHz, in addition to providing the optimum source impedance for the modulators. The use of capacitors which have a large voltage coefficient must be avoided since these will degrade signal linearity. NPO and COG capacitors are acceptable. If active circuitry precedes the ADC, it is recommended that the above RC filter is placed between the active circuitry and the AINR and AINL pins. The above example frequencies scale linearly with sample rate.

High Pass Filter

The operational amplifiers in the input circuitry driving the CS5334/5 may generate a small DC offset into the A/D converter. The CS5334 and CS5335 include a high pass filter after the decimator to remove any DC offset which could result in recording a DC level, possibly yielding "clicks" when switching between devices in a multichannel system. The high pass filter can be disabled with the HP DEFEAT pin. The high pass filter works by continuously subtracting a measure of the dc offset from the output of the decimation filter. If the HP DEFEAT pin is taken high during normal operation, the current value of the dc offset register is frozen and this dc offset will continue to be subtracted from the conversion result. This feature makes it possible to perform a system calibration by;

1. removing the signal source (or grounding the input signal) at the input to the subsystem containing the CS5334/5,
2. running the CS5334/5 with the HP DEFEAT pin low (high pass filter enabled) until the filter settles (approximately 1 second), and
3. taking the HP DEFEAT pin high, disabling the high pass filter and freezing the stored dc offset.

A system calibration performed in this way will eliminate offsets anywhere in the signal path between the calibration point and the CS5334/5.

The characteristics of the first-order high pass filter are outlined below for an output sample rate of 48 kHz. This filter response scales linearly with sample rate.

Frequency response: -3 dB @ 0.9 Hz
-0.01 dB @ 20 Hz
Phase deviation: 2.6 degrees @ 20 Hz
Passband ripple: None

INPUT LEVEL MONITORING

The CS5334 and CS5335 include independent Peak Input Level Monitoring for each channel. The analog-to-digital converter continually monitors the peak digital signal for both channels, prior to the digital limiter, and records these values in the Active registers. This information can be transferred to the Output registers by a high to low transition on the Peak Update pin (PU) which will also reset the Active register. The Active register contains the peak signal level since the previous peak update request.

The 8-bit contents of the output registers are available in all interface modes and are present in the data block as shown in Figure 2. The monitoring function can be formatted to indicate either High Resolution Mode or Bar Graph Mode. The monitoring function is determined on power-up by the presence of a 47 kohm pull-down resistor on FRAME. The addition of a 47 kohm pull-down resistor on the FRAME pin sets the monitoring function to the Bar Graph mode.

High Resolution Mode

Bits P7-P0 indicate the peak input level since the previous peak update (or low transition on the Peak Update pin). If the full scale input level is exceeded (Bit P7 high), bits P5-P0 represent the peak value up to 3 dB above full-scale in 1 dB steps. If the ADC input level is less than full-scale, bits P5-P0 represent the peak value from -60 dB to 0 dB of full scale in 1 dB steps. The PSL outputs are accurate to within 0.25 dB. Bit P6 provides a coarse means of determining an ADC input idle condition. Bit P7 indicates an ADC overflow condition, if the ADC input level is greater than full-scale.

P7 - Overrange

- 0 - Analog input less than full-scale level
- 1 - Analog input greater than full-scale

P6 - Idle channel

- 0 - Analog input >-60 dB from full-scale
- 1 - Analog input <-60 dB from full-scale

P5 to P0 - Peak Signal Level Bits (1 dB steps)

<u>Inputs <0 dB</u>	<u>P5 - P0</u>
0 dB	000000
-1 dB	000001
-2 dB	000010
-60 dB	111100

<u>Inputs >0 dB</u>	<u>P5 - P0</u>
0 dB	000000
+1 dB	000001
+2 dB	000010
+3 dB	000011

Bar Graph Mode

This mode provides a decoded output format which indicates the peak Peak Signal Level in a "Bar Graph" format.

<u>Input Level</u>	<u>P7 - P0</u>
Overflow	11111111
0 dB to -3 dB	01111111
-3 dB to -6 dB	00111111
-6 dB to -10 dB	00011111
-10 dB to -20 dB	00001111
-20 dB to -30 dB	00000111
-30 dB to -40 dB	00000011
-40 dB to -60 dB	00000001
< - 60 dB	00000000

Overflow

Overflow indicates analog input overrange, for both the Left and Right channels, since the last update request on the Peak Update pin. A value of 1 indicates an overrange condition. The left channel information is output on OVFL during the left channel portion of LRCK. The right channel information is available on OVFL during the right channel portion of LRCK.

Initialization

Upon initial power-up, the digital filters and delta-sigma modulators are reset and the internal voltage reference is powered down. The CS5334/5 will remain in the power-down mode until valid clocks are presented. A valid MCLK is required to exit power-down in Master Mode. However, in Slave Mode, MCLK and LRCK of the proper ratio are required to exit power-down. MCLK occurrences are also counted over one LRCK period to determine the MCLK / LRCK frequency ratio in Slave Mode. Power is then applied to the internal voltage reference, the analog inputs will move to approximately 2.2V and output clocks will begin (Master Mode only). This process requires 32 periods of LRCK and is followed by the initialization sequence.

Initialization with High Pass Filter Enabled

28,672 LRCK cycles are required for the initialization sequence with the high pass filter enabled. This time is dominated by the settling time required for the high pass filter.

Initialization and Internal Calibration with High Pass Filter Disabled

If the HP DEFEAT pin is high (high pass filter disabled) during the initialization sequence, the CS5334/5 will perform an internal dc calibration by:

1. disconnecting the internal ADC inputs from the input pins,
2. connecting the (differential) ADC inputs to a common reference voltage,

3. running the high pass filter with a fast settling time constant,
4. freezing the dc offset register, and
5. reconnecting the internal ADC inputs to the input pins.

This procedure takes 4,160 cycles of LRCK. Unlike the system calibration procedure described in the High Pass Filter section, a dc calibration performed during start-up will only eliminate offsets internal to the CS5334/5, and should result in output codes which accurately reflect the differential dc signal at the pins.

Power-Down

The CS5334 and CS5335 have a power-down mode wherein typical consumption drops to 1.0 mW. This is initiated when a loss of clock is detected (either LRCK or MCLK in Slave Mode or MCLK in Master Mode), $\overline{\text{RST}}$ is enabled or DIF0 / DIF1 are at a logic 1. The initialization sequence will begin whenever valid clocks are restored, $\overline{\text{RST}}$ is disabled and DIF0 / DIF1 are restored. If the MCLK / LRCK frequency ratio changes during power-down, the CS5334/5 will adapt to these new operating conditions. However, only the $\overline{\text{RST}}$ method of power-down will include the Master/Slave decision in the initialization sequence.

Grounding and Power Supply Decoupling

As with any high resolution converter, the CS5334 and CS5335 require careful attention to power supply and grounding arrangements to optimize performance. Figure 1 shows the recommended power arrangements with VA+ connected to a clean +5 volt supply. VD+ should be derived from VA+ through a 2 ohm resistor. VD+ should not be used to power additional digital circuitry. All mode pins which require VD+ should be connected to pin 6 of the CS5334/5. All mode pins which require DGND should be connected to pin 5 of the CS5334/5. AGND and DGND, Pins 4 and 5, should be connected together at the CS5334/5. DGND for the CS5334/5 should not be confused with the ground for the digital section of the system. The CS5334/5 should be positioned over the analog ground plane near the digital / analog ground plane split. The analog and digital ground planes must be connected elsewhere in the system. The CS5334/5 evaluation board, CDB5334/5, demonstrates this layout technique. This technique minimizes digital noise and insures proper power supply matching and sequencing. Decoupling capacitors should be located as near to the CS5334/5 as possible.

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C a l l : (5 1 2) 4 4 5 - 7 2 2 2

Digital Filter

Figures 7-10 show the performance of the digital filter included in the CS5334/5. All plots are normalized to F_s . Assuming a sample rate of 48 kHz, the 0.5 frequency point on the plot refers to 24 kHz. The filter frequency response scales precisely with the sample rate.

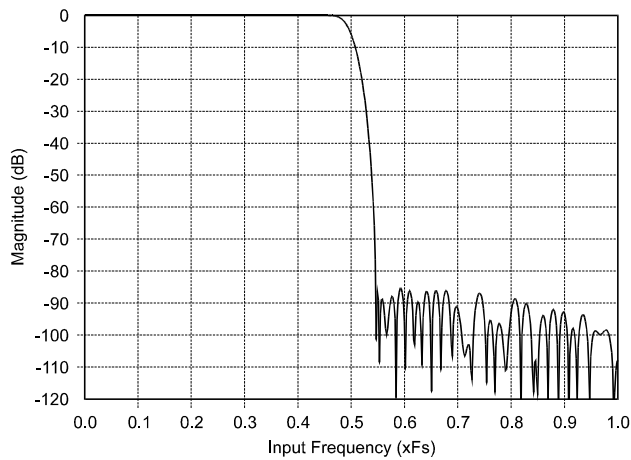


Figure 7. CS5334/5 Digital Filter Stopband Rejection

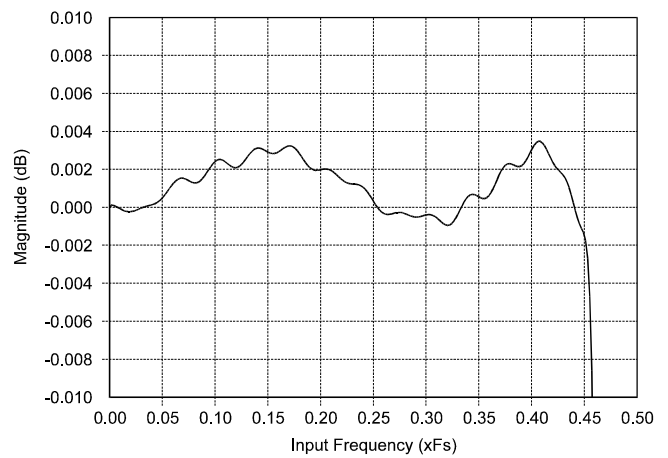


Figure 9. CS5334/5 Digital Filter Passband Ripple

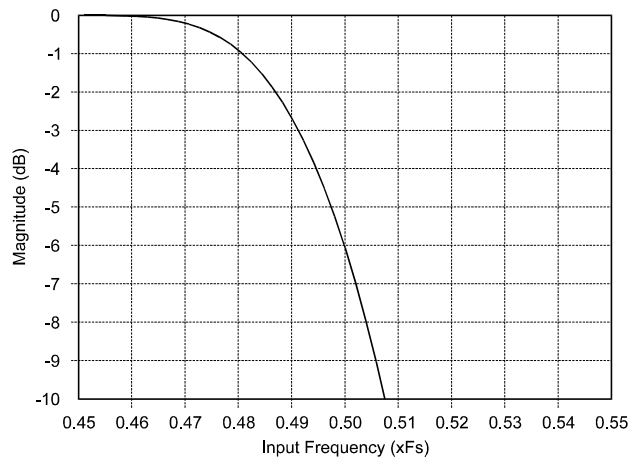


Figure 8. CS5334/5 Digital Filter Transition Band

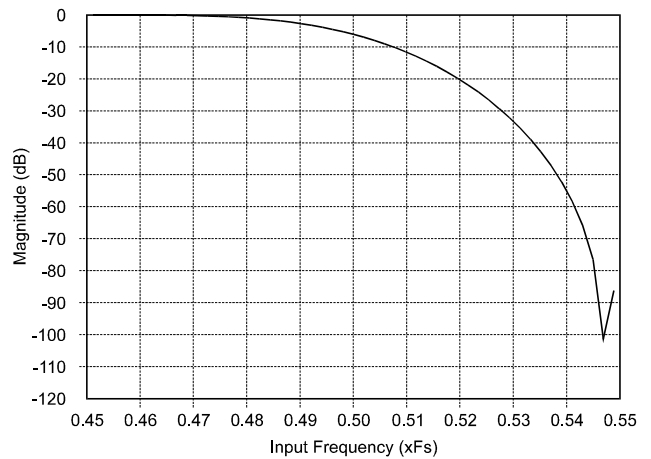


Figure 10. CS5334/5 Digital Filter Transition Band

PIN DESCRIPTIONS

High Pass Filter Defeat	HP DEFEAT	1	20	DIF0	Digital Interface Format 0
OverFlow	OVFL	2	19	DIF1	Digital Interface Format 1
Analog Power	VA+	3	18	RST	Reset
Analog Ground	AGND	4	17	AINL+	Non-Inverting Left Channel Input
Digital Ground	DGND	5	16	AINL-	Inverting Left Channel Input
Digital Power	VD+	6	15	CMOUT	Common Mode Output
Master Clock	MCLK	7	14	AINR-	Inverting Right Channel Input
Serial Data Clock	SCLK	8	13	AINR+	Non-Inverting Right Channel Input
Serial Data Output	SDATA	9	12	LRCK	Left/ Right Clock
Frame Signal	FRAME	10	11	PU	Peak Update

Power Supply Connections

VA+ - Positive Analog Power, Pin 3.

Positive analog supply. Nominally +5 volts.

VD+ - Positive Digital Power, Pin 6.

Positive digital supply. Nominally +5 volts.

AGND - Analog Ground, Pin 4.

Analog ground reference.

DGND - Digital Ground, Pin 5.

Digital ground reference.

Analog Inputs

AINR-, AINR+ - Differential Right Channel Analog Input, Pin 14 and Pin 13.

Analog input connections of the right channel differential inputs. Typically 2 V_{rms} differential (1V_{rms} for each input pin) for a full-scale analog input signal.

AINL-, AINL+ - Differential Left Channel Analog Input, Pin 16 and Pin 17.

Analog input connections of the left channel differential inputs. Typically 2 V_{rms} differential (1V_{rms} for each input pin) for a full-scale analog input signal.

Analog Outputs

CMOUT - Common Mode Output, Pin 15.

This output, nominally 2.2V, can be used to bias the analog input circuitry to the common mode voltage of the CS5334/5.

Digital Inputs

MCLK - Master Clock, Pin 7.

Clock source for the delta-sigma modulator sampling and digital filters.

In Master Mode, the frequency of this clock must be $256\times$ the output sample rate, F_s .

In Slave Mode, the frequency of this clock must be either $256\times$, $384\times$ or $512\times F_s$.

DIF0, DIF1 - Digital Interface Format, Pins 19 and 20.

These two pins select one of 3 digital interface formats or power-down. The format determines the relationship between SCLK, LRCK and SDATA. The formats are detailed in Figures 3-5.

RST - Reset, Pin 18.

A low logic level on this pin activates Reset.

HP DEFEAT - High Pass Filter Defeat, Pin 1.

A high logic level on this pin disables the digital high pass filter. A low logic level on this pin enables the high pass filter.

PU - Peak Update, Pin 11.

Transfers the Peak Signal Level contents of the Active Registers to the Output Registers on a high to low transition on this pin. This transition will also reset the Active register.

Digital Inputs / Outputs

LRCK - Left/Right Clock, Pin 12.

LRCK determines which channel, left or right, is to be output on SDATA. The relationship between LRCK, SCLK and SDATA is controlled by DIF0 and DIF1. Although the outputs for each channel are transmitted at different times, Left/Right pairs represent simultaneously sampled analog inputs. In Master Mode, LRCK is an output clock whose frequency is equal to the output sample rate, F_s . In Slave Mode, LRCK is an input clock whose frequency must be equal to F_s .

SCLK - Serial Data Clock, Pin 8.

Clocks the individual bits of the serial data out from the SDATA pin. The relationship between LRCK, SCLK and SDATA is controlled by DIF0 and DIF1.

In Master Mode, SCLK is an output clock with a frequency of $64\times$ the output sample rate, F_s .

In Slave Mode, SCLK is an input.

Digital Outputs

SDATA - Serial Data Output, Pin 9.

Two's complement MSB-first serial data of 20 bits is output on this pin. Included in the serial data output is the 8-bit Input Signal Level Bits. The data is clocked out via the SCLK clock and the channel is determined by LRCK. The relationship between LRCK, SCLK and SDATA is controlled by DIF0 and DIF1.

OVFL - Overflow, Pin 2.

Overflow indicates analog input overrange, for both the Left and Right channels, since the last update request on the PEAK UPDATE (PU) pin. A value of 1 in the register indicates an overrange condition. The left channel information is output on OVFL during the left channel portion of LRCK. The right channel information is available on OVFL during the right channel portion of LRCK. The registers are updated with a high to low transition on the PEAK UPDATE pin. A 47 kohm pull-down resistor on this pin will set the CS5334/5 in Master Mode.

FRAME - Frame Signal, Pin 10.

Frames the Peak Signal Level (PSL) Bits. FRAME goes high coincident with the leading edge of the first PSL bit and falls coincident with the trailing edge of the last PSL bit as shown in Figures 3-5. A 47 kohm pull-down resistor on this pin will set the Peak Signal Level Monitoring format to "Bar Graph" mode.

PARAMETER DEFINITIONS**Dynamic Range**

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic Range is a signal-to-noise ratio measurement over the specified band width made with a -60dBFS signal. 60dB is added to resulting measurement to refer the measurement to full-scale. This technique ensures that the distortion components are below the noise level and do not effect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307. Expressed in decibels.

Total Harmonic Distortion + Noise (THD+N)

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified band width (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels. Measured at -1 and -20 dBFS as suggested in AES17-1991 Annex A.

Frequency Response

A measure of the amplitude response variation from 10 Hz to 20 kHz relative to the amplitude response at 1 kHz. Units in decibels.

Interchannel Isolation

A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with no signal at the input under test and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch

The gain difference between left and right channels. Units in decibels.

Gain Error

The deviation from the nominal full-scale analog input for a full-scale digital output.

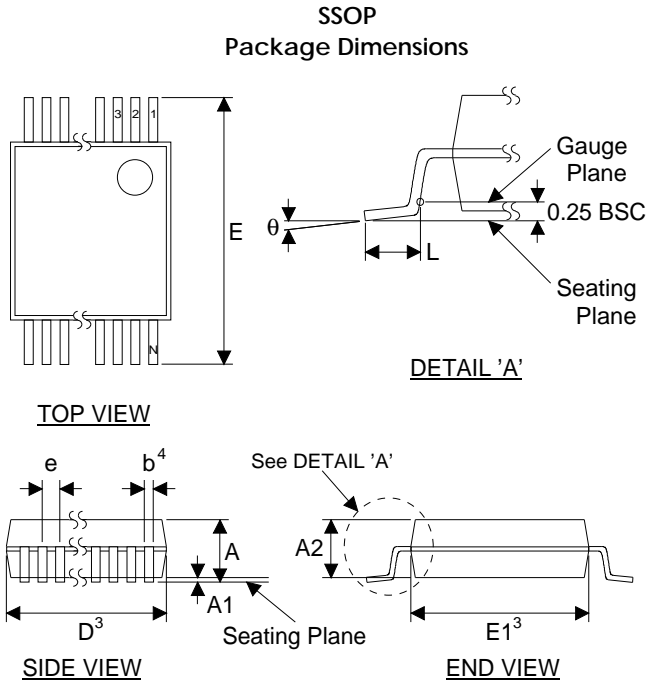
Gain Drift

The change in gain value with temperature. Units in ppm/°C.

Offset Error

The deviation of the mid-scale transition (111...111 to 000...000) from the ideal. Units in mV.

PACKAGE DIMENSIONS



Notes:

1. Dimensioning and tolerance per ANSI.Y14.5M-1982.
2. Symbols are defined in the "MO Series Symbol List" in section 2.2 of JEDEC Publication 95.
3. "D" and "E1" are reference datums and do not include mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20mm per side.
4. Dimension b does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13mm total in excess of b dimension at maximum material condition. Dambar intrusion shall not reduce dimension b by more than 0.07mm at least material condition.
5. These dimensions apply to the flat section of the lead between 0.10 and 0.25mm from lead tips.

DIM	MILLIMETERS			Note
	MIN	NOM	MAX	
A	-	-	2.13	
A1	0.05	-	0.25	
A2	1.62	1.75	1.88	
b	0.22	-	0.38	4, 5
D	see other table			3
E	7.40	7.80	8.20	
E1	5.00	5.30	5.60	3
e	0.65 BSC			
L	0.63	0.90	1.03	
N	see other table			
θ	0°	4°	8°	

N	D			Note
	MIN	NOM	MAX	
8	2.70	3.00	3.30	3
14	5.90	6.20	6.50	3
16	5.90	6.20	6.50	3
18	6.90	7.20	7.50	3
20	6.90	7.20	7.50	3
22	7.90	8.20	8.50	3
24	7.90	8.20	8.50	3
28	9.90	10.20	10.50	3
30	9.90	10.20	10.50	3

• **Notes** •

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